REMARKS

Claims 1-3, 7-14, 17, and 21-25 are pending in the Application. Claims 21-25 are newly added with this amendment. Initially, Applicants wish to thank the Examiner for indicating that the previous rejections have been overcome. Claim 1 has been amended to remove the limitation that the transistor be a CMOS transistor. Amended claim 1 is believed to be allowable because, as described more fully below, the cited art does not teach the presently claimed invention.

Newly added claim 21 is believed to be allowable because it recites the feature of a permeation layer to each unit cell of the array. Newly added claims 22-23 are believed to be allowable because they further provide for the control of the first and second row and column transistors by the first and second row and column selectors, respectively. Similarly, newly added claims 24-25 are believed to be allowable because they further provide for the selection of the first and second row and column transistors by the first and second row and column selectors, respectively.

The claims have been newly rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent No. 5,962,856 (*Zhao et al.*) in view of U.S. Patent No. 5,528,043 (*Spivey et al.*). Applicants respectfully traverse this newly applied rejection.

The presently claimed invention is directed to a circuit for control of an output current in a multiple unit cell array. Specifically, Figure 9 depicts one way in which to implement the claimed invention. The chip includes a multi-site array 210 with electrically repetitive site cell locations. An individual unit cell 212 of the array 210 of unit cells is selected by action of **two** row selectors 220 and 220' and **two** column selectors 230 and 230'. The unit

cell 212 further includes **two** sets of **two** select transistors, namely, a column select transistor and a row select transistor coupled in series.

In operation, the selection registers are sequentially loaded with values indicating selection, or not, of a unit cell 212. The column selector 230 receives an input 232 for determining the selection of a column. The column selector 230 is coupled to the column lines 234 which serve to provide a column select signal 296a-d to the unit cell 212. Additionally, a second row selector 220', input lines 222', second row lines 224' and column contacts 226 are included for activation of the unit cell 212. Likewise, a second column selector 230' is added, having an input 232', and being coupled to secondary or supplemental column lines 234', which in turn are coupled to secondary column contacts 236'.

In contrast, *Zhao et al.* describes a system and circuit for a readout of imaging information comprising an array of capacitors which store charges, the presence or absence of charge depending upon whether radiation existed at the "pixel."

Figures 1A and 1B of *Zhao et al.* show a 3x3 array of pixels and associated readout circuitry. Each cell/pixel couples the capacitor information to the readout circuitry. In operation, the scanning controller selects a first row. A voltage is applied to the gate ("G") for pixels in the row, thereby coupling the pixels to the associate amplifier 22. If the pixel contained a charge, the output of the amplifier is of one state, but if the pixel contained no charge, the output of the amplifier would be of a different state. The multiplexer thereafter provides for selective column readout.

Numerous claim limitations are nowhere taught or suggested in *Zhao et al.* For

example, the claims require **two** supplies, e.g., "a first supply...and a second supply...." And further, in certain embodiments, namely newly added claims 24-25, the invention requires **two** sets of column and row selectors, e.g., "a first column select transistor...a first row select transistor...the first select transistors being connected in series..." and "a second column select transistor...a second column select transistor...the second select transistors being connected in series...."

Zhao et al. is completely different from the presently claimed invention in terms of structure and function. Whereas *Zhao et al.* is designed for the readout of a single bit at each of the pixel locations, Applicants' claimed invention provides for the controlled, selective application of a first supply or a second supply (or both in combination). The readout device described in *Zhao et al.* does not teach – and would have no use for – such a dual supply system.

Spivey et al. does not supply the deficiencies found in *Zhao et al.* to reach the presently claimed invention. Similar to the readout device described in *Zhao et al.*, *Spivey et al.* discloses a system including a detector comprised of a radiation-absorbing layer sandwiched between an array of CMOS integrated circuits and a surface electrode layer transparent to radiation. Discrete distribution of stored voltages across the array proportional to the distribution of radiation photons incident on the absorbing layer are provided. Circuitry in each circuit provides for the voltage on each circuit capacitor to be recorded via readout circuitry. Thus, the arrays described in *Zhao et al.* and *Spivey et al.* are detector arrays and not the actively driven arrays described in the claims of the present invention.

Applicants respectfully request that the Examiner reconsider the claim rejections based on the foregoing discussion of the *Zhao* et al. and *Spivey* et al. references. Applicants believe the pending claims are allowable over the cited art and respectfully request a notice of allowability.

Respectfully submitted,

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